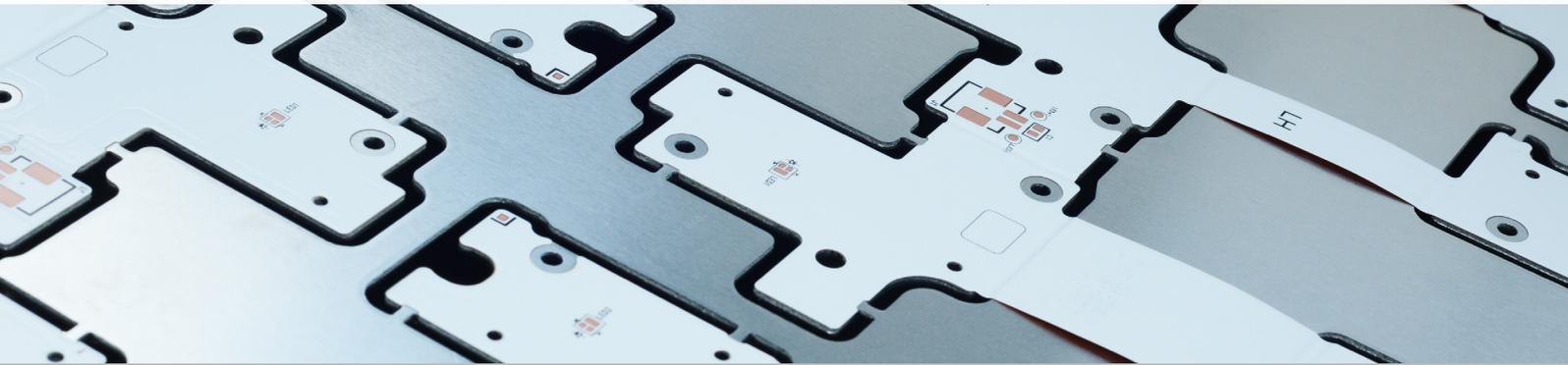


VIA HOLES – MANY WAYS TO CLOSE THEM



INTRODUCTION

You may refer to it as “plugged via”, “tented via”, “filled via” or “covered via” and believe it to be all the same for PCB manufacturers. In reality, there are many processes available for closing vias. However, the right choice depends on the end application. This Knowledge School Doc presents the major benefits of via protection and also the details and restrictions of different related technologies. Remember, if your application doesn’t require closed vias, leave them open! To facilitate a better understanding between PCB designer and PCB manufacturer, the emphasis is placed on understanding the relevant vocabulary. Partner manufacturers of CML can cover most via protection demands. Our capabilities are mentioned under each of the different technologies in this document. For more information, please refer to IPC-4761 standard, Design Guide for Protection of Printed Board Via Structures (July 2006).

BENEFITS OF VIA PROTECTION

Prior to discussing the different via protection methods, we must define “via”. It is a plated through hole with no component soldered into it and usually a diameter of less than 1mm.

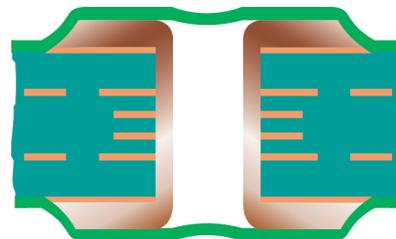
Vias can be “interconnect vias”, used for electrical connection between different PCB layers, or “thermal vias”, used to dissipate heat.

The main reasons for choosing covered vias:

- Prevent bridging between closely spaced holes
- Eliminate solder flow up vias during assembly
- Reduce solder balling
- Minimize flux residues and ionic contamination
- Prevent epoxy resin flowing down holes when encapsulating BGA chips
- Create sufficient vacuum during board handling and/or testing (vacuum seal)
- Prevent conformal coating, also called tropical varnish, flowing down holes
- Ensure planarity of inner core with buried vias

TENTED VIAS WITH DRY-FILM SOLDER MASK

The term “tenting” gained popularity with the use of dry-film solder mask (SM) in PCB manufacturing. The dry-film SM lies across the top of the vias providing a cover or “tent” to protect the vias. There are no apertures on SM layer data and no surface finishing is applied to the via barrel.



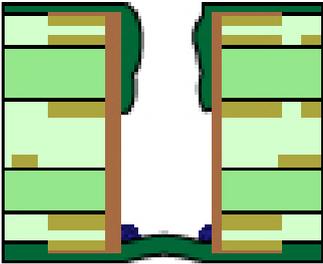
This is the oldest and easiest way to protect vias without additional processes. There is also no cost impact.

In the past, it was standard practice to tent vias with dry-film SM. However, because of cost and quality concerns with today’s fine line technology, dry-film SM is now rarely used, and mainly limited to older military applications.

This technology is not available at CML.

TENTED VIAS WITH LPISM

Today, LPISM (Liquid Photo-Imageable Solder Mask) is a standard SM. Older PCB designs without apertures on the SM layer lead to “tented” vias as shown below:



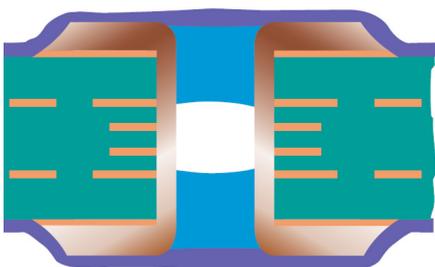
There are three common methods of applying LPISM: curtain, spray and screen coating. Curtain coating tents smaller holes (about 0.3mm and below) but by no means is it reliable. Tenting capability with spray coating is almost non-existent. Tenting by screen coatings is limited by the hole size and the surface tension of the liquid mask.

Risk: If a via is not tented on both sides, entrapments of chemicals from processes after solder mask are probable. For instance, all the finishes are subjected to a micro-etch process. The micro-etchant that gets trapped in the capped via will crystallize rapidly to form copper salt crystals. Over time, these crystals can cause long-term reliability issues. In the case of ENIG finish, the gold and small area of exposed copper near the cap forms a galvanic cell, which in turn accelerates the etch process.

At CML: LPI SM is applied by screen printing and is capable of “tenting” very small vias (max 0.3mm). For bigger vias, we recommend adding apertures on the SM layer in order to cover via pads with SM and keep the via open (*size of aperture = finished hole size - 0.15mm*).

PLUGGED AND COVERED VIAS

Vias are plugged with solder mask (STEP 1). Then standard LPISM is applied over the plug (STEP 2). Plugging data needs to indicate which vias are to be plugged. Also, no surface finish is applied to the via barrel.



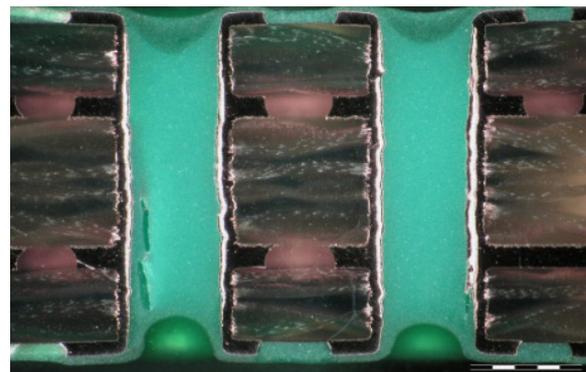
This process was developed as a modification of the LPISM tent and has a moderate cost impact. The process is restricted by the via size and is best suited for vias with a finished diameter of 0.4 to 0.5mm.

Plugging can be done either from one side (usually the bottom side) or from both sides. Plugging from both sides as shown above can prove to be a tricky process. During the curing step, the heated air entrapped inside the hole may expand and cause a “blow out”, resulting in cracked or broken plugs.

With a single-sided plugging process, it is common and perfectly acceptable to have partially filled vias - meaning the SM does not come completely to the top of the hole. A quick inspection to ensure that light does not pass through via is all that is required for a hole to be considered plugged.

After plugging, via holes are covered on one or both sides with SM.

At CML: We recommend plugged vias covered with SM on both sides. This technology is available with all types of finishings for via diameters of 0.4mm to 0.5mm.

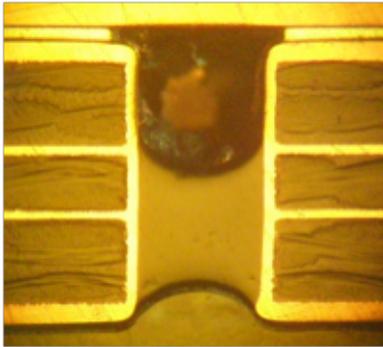


Cross-section (plugged and 2-sided covered vias)



View from top (plugged and 2-sided covered vias)

For some applications, only single sided plugging is required. For thermal vias, for example, component bodies are soldered onto the PCB in order to improve heat dissipation.



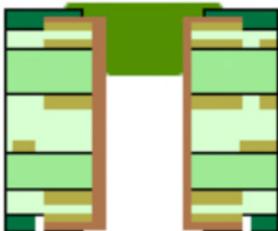
Cross-section (plugged and 1-sided covered vias)

At CML: We recommend the application of ENIG and OSP finishing. With LF HAL, there is a risk that solder will remain inside the vias and create solder balls during the assembly process on PCBA. With Immersion Tin, there is a risk that chemical residues from the immersion tin line will remain inside the vias, and potentially oxidize the copper barrel.

PLUGGING VIAS AFTER FINAL SURFACE APPLICATION

Vias are plugged on one side by a second or subsequent solder mask application. The final surface finish is applied to the board and the via barrel prior to the plugging process.

This process is an alternative for plugged and single-side covered vias. It also has a moderate cost impact.



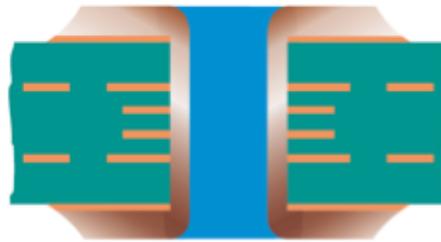
Post surface finish application, an additional mask application process is required. Therefore it is not suitable for OSP or Tin finish.

With this process, the SM height above copper can be relatively high. This can cause a problem during solder paste printing and therefore plugged vias should not be in close proximity to fine pitch components.

At CML: Available upon request.

FILLED VIAS

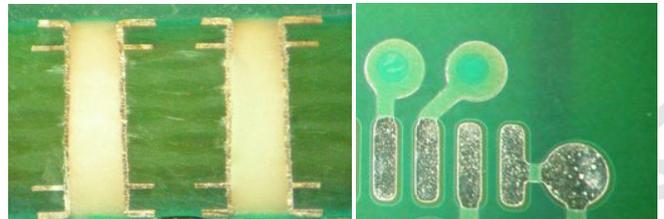
Vias are 100% filled with non-conductive material, usually epoxy resin.



This process is complex and expensive.

Process Flowchart:

- Drill holes
- Metalize holes: Chemical copper followed by electrolytic copper to achieve 20 or 25µm min copper thickness inside holes
- Fill / plug vias with resin: Oxidation, pretreatment, resin plugging, baking (145°C for 30min), abrading, and final baking (145°C for 60min)
- Make outer layer: Laminate, expose, develop photoresist and etch copper
- Continue with SM process, finishing, routing etc.



Vias filled with resin and covered with SM on both sides

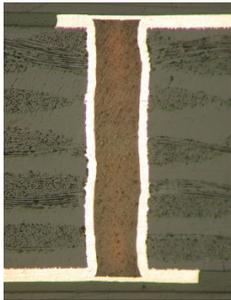
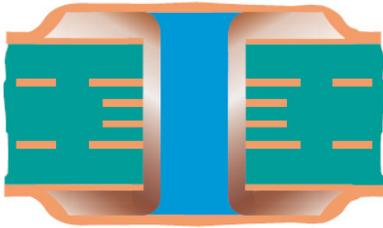
At CML: This process is available but it is costly. The maximum via size permitted is 0.8mm. We recommend this process for multilayers with buried cores.



Cross-section (8-layers HDI PCB with buried 6-layers core)

FILLED AND CAPPED VIAS

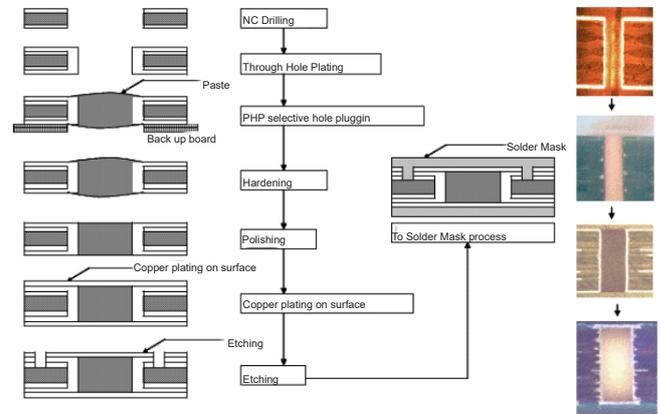
Vias are plugged with a conductive or non-conductive media, planarized and plated over.



This process allows the use of via capture pads as SMT pads. It reduces routing issues on external layers and minimizes inductance.

In addition to the dual plating processes, multiple additional process steps are required. The extra plating process has a negative effect on the minimum feature size capable on the external layers.

VIP Process Flow



Source: Article « Non Conductive Epoxy Filled Vias in PCB's Provides New Product Offerings» from David Hoover (Multek) 05-25-04

At CML: This expensive process is available but we recommend it for via in pad applications only.

THE BOTTOM LINE

It is very cost effective if your PCB does not need plugging, filling or capping.

But for different reasons it might be necessary to protect interconnect vias or thermal vias. In the past, via protection was done by tenting them with dry film SM. This was an easy, cheap and effective method. But as liquid LPI SM began replacing dry film SM, this tenting process was not possible anymore.

Alternative technologies were developed, such as “plugging before SM” (vias are plugged with SM and then covered on one or both sides with SM) or “plugging after finishing”. These technologies face many restrictions, mostly revolving around via size and surface finishing.

Consequently, a high-tech technology emerged: filled vias with resin. This technology has the highest plugging reliability and is recommended for situations such as multilayers with buried cores or for via-in-pad design.